Image

OIPE JC-25 JUL 2 9 2005

TRANSMITTAL FORM	**Application Number**	09/737,743
	Filing Date	12/18/2000
to be used for all correspondence after initial filing	**First Named Inventor**	Sehat SUTARDJA
	Group Art Unit	2631
* Plus ONE Box of Cited References	**Examiner Name**	Phuong M. Phu
Total number of pages in this submission including transmittal **10 ***	**Attorney Docket Number**	MP0020

ENCLOSURES *(check all that apply)*

☐ Fee Transmittal Form	☐ Assignment Papers *(for an Application)*	☐ After Allowance Communication to TC
☐ Fee Attached - Credit Authorization	☐ Drawing(s)	☐ Appeal Communication to Board of Appeals and Interferences
☐ Amendment / Reply	☐ Licensing-related Papers	☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
☐ After Final	☐ Petition	☐ Proprietary Information
☐ Affidavits/declaration(s)	☐ Petition to Convert to a Provisional Application	☐ Status Letter
☐ Extension of Time Request	☐ Power of Attorney, Revocation Change of Correspondence Address	☐ Other Enclosure(s) (identify below):
☐ Express Abandonment Request	☐ Terminal Disclaimer	
☑ Information Disclosure Statement *with PTO 1449 Forms and 126 cited references*	☐ Request for Refund	
☐ Certified Copy of Priority Document(s)	☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	
☐ Response to Missing Parts/ Incomplete Application	**REMARKS**	
☐ Response to Missing Parts under 37 CFR 1.52 or 1.53		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	KATTEN MUCHIN ROSENMAN, LLP	
Signature	*Andrew J. Bateman*	
Printed Name	Andrew J. Bateman	
Reg. No.	45,573	Date: 07/29/2005

CERTIFICATE OF FACSIMILE TRANSMISSION OR MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO via fax no. (703) 872-9306 or is being deposited with the US Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	
Typed or Printed Name	Date:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)

    Sehat SUTARDJA, et al.   ) Examiner: Phuong M. Phu

Application No.: 09/737,743   ) Group Art Unit: 2631

Filed: December 18, 2000   ) Confirmation No.: 1406

For: ACTIVE REPLICA TRANSFORMER   )
        HYBRID   Date: July 29, 2005

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

    In compliance with the duty of disclosure under 37 CFR § 1.56 and the requirements of M.P.E.P. § 2001.06(c), and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449s and to copies of any literature and non-U.S. patent documents submitted herewith.

    In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.
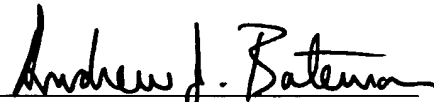
    It is respectfully requested that the information listed on the PTO-1449s be considered by the Examiner, and that an initialed copies be returned indicating that such information was considered.

    No fee is necessary for the submission of this Information Disclosure Statement.

    Should the Examiner have any questions, Applicant's undersigned attorney is reachable by telephone in our Washington, D.C. office at (202) 625-3547. The correspondence address of record is provided below.

Respectfully submitted,

KATTEN MUCHIN ROSENMAN, LLP

By: _____
        Andrew J. Bateman
        Attorney for Applicants
        Registration No. 45,573

IP Docket
Katten Muchin Rosenman, LLP
1025 Thomas Jefferson St., NW
East Lobby, Suite 700
Washington, DC 20007-5201
Facsimile No.: (202) 298-7570
Customer No.: 28285

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743

LIST OF REFERENCES CITED BY APPLICANT

APPLICANT	
Sehat SUTARDJA	

DATE SUBMITTED TO USPTO: July 29, 2005

FILING DATE	GROUP
12/18/2000	2631

FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT
		06-97831	04/08/1994	Japan			with Translation
		05-064231 A	03/12/1993	Japan			Abstract
		09-55770	08/17/1995	Japan			with Translation
		09-270707	03/03/1996	Japan			with Translation
		2001-177409	12/16/1999	Japan			with Translation

OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

	·	Hellwarth, et al., "Digital-to-analog Converter having Common-mode Isolation and Differential Output".
	·	Sedra et al., Microelectronic Circuits, Third Edition, 1991, pp. 48-115.
		Lee, et al., " A CMOS Serial Link for Fully Duplexed Data Communication", April, 1995.
		Shoval et al., "WA 18.7 – A Combined 10/125 Mbaud Twisted-Pair Line Driver with Programmable Performance/Power Features," 2000, pp. 314-315.
	·	Song, et al., "FP 12.1: NRZ Timing Recovery Technique for Band-Limited Channels (Slide Supplement), 1996.
		Chien, "Monolithic CMOS Frequency Synthesizer for Cellular Applications", March 12-13.
		Chien, "Delay Based Monolithic CMOS Frequency Synthesizer for Portable Wireless Applications", May 20, 1998.
	·	Chien, "Low-Noise Local Oscillator Design Techniques using DLL-based Frequency Multiplier for Wireless Applications", 2000.
		Cho et al.; "A Single-Chip CMOS Direct Conversion Transceiver for 900 MHz Spread-Spectrum Digital Cordless Telephones"; 1999
		Shoval et al.; "A CMOS Mixed-Signal 100Mb/s Receive Architecture for Fast Ethernet"; 1999
		Hester et al.; "CODEC for Echo-Canceling Full-Rate ADSL Modems"; December, 1999
		Nack, et al., "A Constant Slew Rate Ethernet Line Driver", May, 2001.
		Song, "Dual Mode Transmitter with Adaptively Controlled Slew Rate and Impedance Supporting Wide Range Data Rates", 2001.
		Yee et al., An Integratable 1-2.5 Gbps Low Jitter CMOS Transceiver with Built in Self Test Capability, 1999
		Intersil, HC-5509B ITU CO/Loop Carrier SLIC, 8/2003
		Regan, ADSL Line Driver/Receiver Design Guide, Part 1, 2/2000
		Phillps, The HC-5502X14X Telephone Subscriber Line Interface Circuits (SLIC), 1/1997
		Fuad Surial Atiya, et al., An Operational Amplifier Circulator Based on the Weighted Summer, 6/1975

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743

LIST OF REFERENCES CITED BY APPLICANT

APPLICANT	
Sehat SUTARDJA	

DATE SUBMITTED TO USPTO: July 29, 2005

FILING DATE	GROUP
12/18/2000	2631

OTHER DOCUMENTS

		Narayanan et al., Doppler Estimation Using a Coherent Ultrawide-Band Random Noise Radar, 6/2000
		Stephens, Active Output Impedance for ADLS Line Drivers, 11/2002
		Hellums et al., An ADSL Integrated Active Hybrid Circuit
		Azadet et al., A Gigabit Transceiver Chip Set for UTP CA-6 Cables in Digital CMOS Technology, 2/2000
		He et al., A DSP Receiver for 1000 Base-T PHY, 2001
		Baird et al., A Mixed Sample 120M s PRML Solution for DVD Systems, 1999
		Baker, An Adaptive Cable Equalizer for Serial Digital Rates to 400Mb/s, 1996
		Everitt et al., A 10/100Mb/s CMOS Ethernet Transceiver for 10BaseT, 10BaseTX and 100Base FX, 1998
		Roo et al., A CMOS Transceiver Analog Front-end for Gigabit Ethernet over Cat-5 Cables, 2001
		Shoaei et al., A 3V Low Power 0.25um CMOS 100Mb/s Receiver for Fast Ethernet, 2000
		Walker et al., A Two Chip 1.5 GBd Serial Link Interface, 12/1992
		Chien, et al., "TP 12.4: A 900-MHz Local Oscillator using a DLL-based Frequency Multiplier Technique for PCS Applications".
		Lee, et al., "A 3V 10b 100 MS/s Digital-to-Analog Converter for Cable Modem Applications, August 28-30, 2000 pp. 203-205.
		Rudell, et al., "SA 18.3: A 1.9 GHz Wide-band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications," 1997, pp. 304-305, 476.
		Young, et al., "Monolithic High-Performance three-Dimensional Coil Inductors for Wireless Communications, 1997
		Wu, et al., "A low glitch 10-bit 75 MHz CMOS video D/A converter, January 1995, pp. 68-72

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO.	APPLICATION NO.
	MP0020	09/737,743

LIST OF REFERENCES CITED BY APPLICANT	APPLICANT
	Sehat SUTARDJA

DATE SUBMITTED TO USPTO: July 29, 2005	FILING DATE	GROUP
	12/18/2000	2631

FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT
		63-300700	07/12/1988	Japan			Abstract
		06-029853	02/04/1994	Japan			Abstract
		62-159925	7/15/87	Japan			with Translation
		6-276182	9/30/94	Japan			with Translation

OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

	Johns, et al., "Integrated Circuits for Data Transmission Over Twisted Pair Channels", March, 1997, pgs. 398-406.
	"IEEE Standard 802.3: Part 3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Detection", March 8, 2002, pages 1-1538
	Young, et al., "A Low-Noise RF Voltage-Controlled Oscillator Using On-Chip High-Q Three-Dimensional Coil Inductor and Micromachined Variable Capacitor", June 8-11, 1998, pgs. 128-131.
	Young, et al., "A Micromachined Variable Capacitor for Monolithic Low-Noise VCOS", 1996, pgs. 86-89.
	Abidi, et al., "FA 7.2: The Future of CMOS Wireless Transceivers", February 7, 1997, pgs. 118-119, 440.
	Eto, et al., "A 333 MHz, 20mW, 18ps Resolution Digital DLL using Current-controlled Delay with Parallel Variables Resistor DAC (PVR-DAC)", August 28-30, 2000, pgs. 349-350.
	Ivan Jorgensen, et al., "Design of a 10-bit 100 MSamples/s BiCMOS D/A Converter", 1996, pgs. 730-733.
	Henriques, et al., "A CMOS Steering-Current Multiplying Digital-to-Analog Converter", 1995, pgs. 145-155.
	Wikner, et al., "Modeling of CMOS Digital-to-Analog Converters for Telecommunication", May, 1999, pgs. 489-499.
	Van der Plas, et al., "A 14-Bit Intrinsic Accuracy Q^2 Random Walk CMOS DAC", December, 1999, pgs. 1708-1718.
	Radke, et al., "A 14-Bit Current-Mode $\Sigma\Delta$ DAC Based Upon Rotated Data Weighted Averaging", August, 2000, pgs. 1074-1084.
	Shui, et al., "Mismatch Shaping for a Current-Mode Multibit Delta-Sigma DAC", March, 1999, pgs. 331-338.
	Hamasaki, et al., "A 3-V, 22-mV Multibit Current-Mode $\Sigma\Delta$ DAC with 100 dB Dynamic Range", December, 1996, pgs. 1888-1894.
	Van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters – Chapter 6, pgs. 211-271.
	Millman, et al., "Pulse, Digital, and Switching Waveforms", pgs. 674-675.
	Tsutomu Kamoto, "An 8-bit 2-ns Monolithic DAC", February, 1988.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. MP0020	APPLICATION NO. 09/737,743
LIST OF REFERENCES CITED BY APPLICANT	**APPLICANT** Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 29, 2005	**FILING DATE** 12/18/2000	**GROUP** 2631

FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

	Weaver, Jr., "A Third Method of Generation and Detection of Single-Sideband Signals," December 1956, pp. 1703-1705.
	Niknejad et al., "Analysis and Optimization of Monolithic Inductors and Transformers for RF ICs," 1997, pp. 375-378.
	Weigandt et al., "Analysis of Timing Jitters in CMOS Ring Oscillators," pp. 27-30.
	Niknejad et al., "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC's," October 1998, pp. 1470-1481.
	American National Standard, "Fibre Distributed Data Interface (FDDI) – Token Ring Twisted Pair Layer Medium Dependent (TP-PMD)," September 25, 1995.
	Nguyen et al., "Si IC-Compatible Inductors and LC Passive Filters," August 1990, pp. 1028-1031.
	Gardner, "Charge-Pump Phase-Lock Loops," November 1980, pp. 1849-1858.
	Dally et al., "High Performance Electrical Signaling."
	Davies, "Digital Generation of Low-Frequency Sine Waves," June 1969, pp. 97-105.
	Abidi, "TP 11.1: Direct-Conversion Radio Transceivers for Digital Communications," 1995.
	Dolle, "A Dynamic Line-Termination Circuit for Multireceiver Nets," December 1993, pp. 1370-1373.
	Su et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," April 1993, pp. 420-430.
	Gray et al., "Future Directions in Silicon ICs for RF Personal Communications," 1995, pp. 83-90.
	Gabara, "On-Chip Terminating Registers for High Speed ECL-CMOS Interfaces," 1992, pp. 292-295.
	Horowitz et al., "High-Speed Electrical Signaling: Overview and Limitations," 1998, pp. 12-24.
	Efendovich et al., Multifrequency Zero-Jitter Delay-Locked Loop, 1/1994, 67-70
	Munshi et al., Adaptive Impedance Matching, 69-72
	Niknejad et al., Numerically Stable Green Function for Modeling and Analysis of Substrate Coupling in Integrated Circuits, 4/1998, 305-315
	Hajimiri et al., Phase Noise in Multi-Gigahertz CMOS Ring Oscillators, 1998, 49-52
	Kim et al., PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design, 31-34

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

	Kim et al., "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2-μm CMOS," 1990, pp. 1385-1394.	
	Liu et al., "WP 23.7: A 6.5 GHz Monolithic CMOS Voltage-Controlled Oscillator," 1999, pp. 404-405, 484.	
	Wang et al., "WP 23.8: A 9.8 GHz Back-Gate Tuned VCO in 0.35 μm CMOS," 1999, pp. 406-407, 484.	
	Rofougaran et al., "SP 24.6: A 900 MHz CMOS LC-Oscillator with Quadrature Outputs," 1996.	
	Koullias et al., "TP 9.2: A 900 MHz Transceiver Chip Set for Dual-Mode Cellular Radio Mobile Terminals," 1993, pp. 140-141, 278.	
	Dauphinee et al., "SP 23.7: A Balanced 1.5 GHz Voltage Controlled Oscillator with an Integrated LC Resonator," 1997, pp. 390-391, 491.	
	Banu et al., "A BiCMOS Double-Low-IF Receiver for GSM," 1997, pp. 521-524.	
	Chang et al., "A CMOS Channel-Select Filter for a Direct-Conversion Wireless Receiver," 1996, pp. 62-63.	
	Waizman, "FA 18.5: A Delay Line Loop for Frequency Synthesis of De-Skewed Clock," February 18, 1994, pp. 298-299.	
	Kinget, "FP 14.7: A Fully Integrated 2.7V 0.35μm CMOS VCO for 5 GHz Wireless Applications," February 5, 1998.	
	Lee et al., "A Fully Integrated Low-Noise 1-GHz Frequency Synthesizer Design for Mobile Communication Application," May 1997, pp. 760-765.	
	Parker et al., "A Low-Noise 1.6-GHz CMOS PLL with On-Chip Loop Filter," 1997, pp. 407, 409-410.	
	Park et al., "A Low-Noise, 900-MHz VCO in 0.6μm CMOS," May 1999, pp. 586-591.	
	Soyuer et al., "A Monolithic 2.3-Gb/s 100-mW Clock and Data Recovery Circuit in Silicon Bipolar Technology," December 1993, pp. 1310-1313.	
	Hu et al., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2-μm CMOS," December 1993, pp. 1314-1320.	
	Parameswaran et al., "A New Approach for the Fabrication of Micromechanical Structures," December 6, 1998, pp. 289-307.	
	Knight, Jr. et al., A Self-Terminating Low-Voltage Swing CMOS Output Driver, 1988, 457-464	
	Maneatis, Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques, 11/1996, 1723-1732	
	Chang et al., Large Suspended Inductors on Silicon and Their Use in a 1-um CMOS RF Amplifier, 5/1993, 246-248	
	Gharpurey et al., Modeling and Analysis of Substrate Coupling in Integrated Cicuits, 3/1996, 344-353	

EXAMINER	DATE CONSIDERED

ATTORNEY DOCKET NO.	APPLICATION NO.
MP0020	09/737,743

LIST OF REFERENCES CITED BY APPLICANT

APPLICANT
Sehat SUTARDJA

DATE SUBMITTED TO USPTO: July 29, 2005

FILING DATE	GROUP
12/18/2000	2631

FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT

OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

		Shoval et al., "WA 18.7 – A Combined 10/125 Mbaud Twisted-Pair Line Driver with Programmable Performance/Power Features," 2000, pp. 314-315.
		Myson Technology, "MTD214 – Ethernet Encoder/Decoder and 10BaseT Transceiver with Built-in Waveform Shaper," 1997, pp. 1-11.
		Myson Technology, "MTD972 (Preliminary) 100BaseTX PCS/PMA," 1997, pp. 1-21.
		Craninckx et al., "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," 1997, pp. 736-744.
		Craninckx et al., "A 1.8-GHz Low-Phase-Noise Voltage-Controlled Oscillator with Prescaler," 1995, pp. 1474-1482.
		Hung et al., "A 1.24-GHz Monolithic CMOS VCO with Phase Noise of 137 dBc/Hz at a 3-MHz Offset," 1999, pp. 111-113.
		Rudell et al., "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," 1997, pp. 2071-2088.
		Lin et al., "TP 12.5: A 1.4 GHz Differential Low-Noise CMOS Frequency Synthesizer using a Wideband PLL Architecture," 2000, pp. 204-205, 458.
		Razavi, "SP 23.6: A 1.8 GHz CMOS Voltage-Controlled Oscillator," 1997, pp. 388-389.
		Dec et al., "MP 4.8: A 1.9 GHz Micromachine-Based Low-Phase-Noise CMOS VCO," 1999, pp. 80-81, 449.
		Sato et al., "SP 21.2: A 1.9 GHz Single-Chip IF Transceiver for Digital Cordless Phones," February 10, 1996.
		Lee et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabytes/s DRAM," 1994, pp. 1491-1496.
		Joo Leong Tham, et al., "A 2.7-V 900-MHz/1.9-GHz Dual-Band Transceiver IC for Digital Wireless Communication," 1999, pp. 286-291.
		Lam et al., "WP 23.6: A 2.6 GHz/5.2 GHz CMOS Voltage-Controlled Oscillator," 1999, pp. 402-403, 484.
		Marshall et al., "TA 8.7: A 2.7V GSM Transceiver ICs with On-Chip Filtering," 1995.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO. MP0020	APPLICATION NO. 09/737,743
LIST OF REFERENCES CITED BY APPLICANT		**APPLICANT** Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 29, 2005		**FILING DATE** 12/18/2000	**GROUP** 2631

OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

		Rudell et al., Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems, 1998, 149-154
		Shoval et al., A 100 Mb/s BiCMOS Adaptive Pulse-Shaping Filter, 12/1995, 1692-1702
		Jansen et al., SP 23.8: Silicon Bipolar VCO Family for 1.1 to 2.2 GHz with Fully-Integrated Tank and Tuning Circuits, 2/8/1997, 392-393 & 492
		Cho et al.; "A Single-Chip CMOS Direct Conversion Transceiver for 900 MHz Spread-Spectrum Digital Cordless Telephones"; 1999
		LIBERALI ET AL., "Progress in High-Speed and High –Resolution CMOS Data Converters", September 12-14, 1995, pages 19-28
		SEDRA et al., "Micro-Electronic Circuits", 1982, pages 95-97 and 243-247
		DP83220 CDL ™ Twisted Pair FDDI Transceiver Device", October 1992
		MIKI ET AL., "An 80-MHz 8-bit CMOS D/A Converter", December 1986, pages 983-988
		LETHAM ET AL., "A high-performance CMOS 70-Mhzpalette/DAC", December 1987, pages 1041-1047
		NAKAMURA ET AL., "A 10-b 70-MS/s CMOS D/A/ converter", April 1991, pages 637-642
		TAKAKURA ET AL., "A10 bit 80 MHz glitchless CMOS D/A/ converter", May 1991, pages 26.5.1-26.5.4
		FOURNIER ET AL., "A 130-MHz 8-b CMOS video DAC for HDTV applications", July 1991, pages 1073-1077
		REYNOLDS, "A 320 MHz CMOS triple 8b DAC with on-chip PLL and hardware cursor", February 1994, pages 50-51
		CHIN ET AL., "A 10-b 125 MHz CMOS digital-to-analog (DAC) with threshold-voltage compensated current sources", November 1994, pages 1374-1380
		The Authoritative Dictionary of IEEE Standards Stems 7th Edition, page 280
		Chan, et al., "A 100 Mb/s CMOS 100Base-T3 Fast Ethernet Transceiver for Category 3, 4, & 5 UTP, 1998
		WANG, et al., "A 1.2 GHz programmable DLL-Based Frequency Multiplier for Wireless Applications, December 2004

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE			ATTORNEY DOCKET NO. MP0020	APPLICATION NO. 09/737,743
LIST OF REFERENCES CITED BY APPLICANT			**APPLICANT** Sehat SUTARDJA	
DATE SUBMITTED TO USPTO: July 29, 2005			**FILING DATE** 12/18/2000	**GROUP** 2631

U.S. PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
		4,503,421	03/05/1985	HARAYAMA			
		6,295,012	09/25/2001	GREIG			
		6,476,746	11/05/2002	VISWANATHAN			
		6,864,726	03/2005	LEVIN, et al.			

FOREIGN PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION OR ABSTRACT (Yes or No)

OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.